

CLAIMS

What is claimed is:

- 5 1. a method of forming a dual damascene via, said method comprises:
- providing a wafer, wherein said wafer comprises a first metal layer;
- forming a cap layer on said first metal layer;
- 10 forming a first dielectric constant dielectric layer on said cap layer;
- forming a middle etching stop layer on said first dielectric constant dielectric layer;
- forming a second dielectric constant dielectric layer on said
- 15 middle etching stop layer;
- forming a dielectric hard mask layer on said second dielectric constant dielectric layer
- forming a second metal layer on said dielectric hard mask layer;
- removing said partial second metal layer to form a metal hard
- 20 mask layer on said partial dielectric hard mask layer;
- forming a photo mask layer on said second metal layer and said partial dielectric hard mask layer;
- removing said partial dielectric hard mask layer and said partial second dielectric constant dielectric layer to form a first trench in said
- 25 dielectric hard mask layer and said second dielectric constant dielectric layer;
- removing said photo mask layer;
- removing said middle etching stop layer which is at a bottom of

said first trench and said partial dielectric hard mask layer;

removing said partial second dielectric constant dielectric layer
to form a second trench in said second dielectric constant dielectric layer
and removing said partial first dielectric constant dielectric layer to form
5 a third trench in said first dielectric constant dielectric layer, wherein
said second trench and said third are connected with each other;

removing said cap layer which is at a bottom of said third trench
and removing said middle etching stop layer which is at a partial bottom
of said second trench;

10 forming a third metal layer on said second metal layer and in
said second trench and said third trench and filling of said second
trench and said third trench; and

removing said partial third metal layer to expose said second
metal layer and making a surface of said third metal layer and said metal
15 layer become a planar surface.

2. The method according to claim 1, wherein said second
metal layer is titanium.

20 3. The method according to claim 1, wherein said second
metal layer is titanium nitride.

4. The method according to claim 1, wherein said second
metal layer is tantalum.

25 5. The method according to claim 1, wherein said second
metal layer is tantalum nitride.

6. The method according to claim 1, wherein said second metal layer is aluminum.

7. The method according to claim 1, wherein said second
5 metal layer is tungsten.

8. The method according to claim 1, wherein said middle etching stop layer is silicon nitride.

10 9. The method according to claim 1, wherein said middle etching stop layer is silicon carbon.

10. a method of forming a dual damascene via, said method comprises:

15 providing a wafer, wherein said wafer comprises a first metal layer;

forming a cap layer on said first metal layer;

forming a first dielectric constant dielectric layer on said cap layer;

20 forming a middle etching stop layer on said first dielectric constant dielectric layer;

forming a second dielectric constant dielectric layer on said middle etching stop layer;

25 forming a dielectric hard mask layer on said second dielectric constant dielectric layer

forming a second metal layer on said dielectric hard mask layer;

removing said partial second metal layer to form a metal hard mask layer on said partial dielectric hard mask layer;

forming a bottom anti-reflective coating on said second metal layer and said partial dielectric hard mask layer;

forming a photo mask layer on said bottom anti-reflective coating;

5 removing said partial dielectric hard mask layer and said partial second dielectric constant dielectric layer to form a first trench in said dielectric hard mask layer and said second dielectric constant dielectric layer;

10 removing said bottom anti-reflective coating and said photo mask layer;

removing said middle etching stop layer which is at a bottom of said first trench and said partial dielectric hard mask layer;

15 removing said partial second dielectric constant dielectric layer to form a second trench in said second dielectric constant dielectric layer and removing said partial first dielectric constant dielectric layer to form a third trench in said first dielectric constant dielectric layer, wherein said second trench and said third are connected with each other;

20 removing said cap layer which is at a bottom of said third trench and removing said middle etching stop layer which is at a partial bottom of said second trench;

forming a barrier layer on said second metal layer, said partial bottom of said second trench, a sidewall of said second trench, said bottom of said third trench, and a sidewall of said third trench;

25 forming a third metal layer on said barrier layer and in said second trench and said third trench and filling of said second trench and said third trench; and

removing said partial third metal layer to expose said second metal layer and making a surface of said third metal layer and said metal

layer become a planar surface.

11. The method according to claim 10, wherein said second metal layer is titanium.

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12. The method according to claim 10, wherein said second metal layer is titanium nitride.

10 13. The method according to claim 10, wherein said second metal layer is tantalum.

14. The method according to claim 10, wherein said second metal layer is tantalum nitride.

15 15. The method according to claim 10, wherein said second metal layer is aluminum.

16. The method according to claim 10, wherein said second metal layer is tungsten.

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17. The method according to claim 10, wherein said middle etching stop layer is silicon nitride.

25 18. The method according to claim 10, wherein said middle etching stop layer is silicon carbon.

19. The method according to claim 10, wherein a material of said third metal layer is copper.

20. The method according to claim 10, wherein said barrier layer is tantalum nitride/tantalum.

21. The method according to claim 10, wherein said barrier
5 layer is titanium nitride/titanium.

22. a method of forming a dual damascene via, said method comprises:

10 providing a wafer, wherein said wafer comprises a first metal layer;
forming a cap layer on said first metal layer;
forming a first dielectric constant dielectric layer on said cap layer;
forming a middle etching stop layer on said first dielectric
15 constant dielectric layer;
forming a second dielectric constant dielectric layer on said middle etching stop layer;
forming a dielectric hard mask layer on said second dielectric constant dielectric layer
20 forming a second metal layer on said dielectric hard mask layer;
removing said partial second metal layer to form a metal hard mask layer on said partial dielectric hard mask layer;
forming a bottom anti-reflective coating on said second metal layer and said partial dielectric hard mask layer;
25 forming a photo mask layer on said bottom anti-reflective coating;
removing said partial dielectric hard mask layer and said partial second dielectric constant dielectric layer to form a first trench in said

dielectric hard mask layer and said second dielectric constant dielectric layer;

removing said bottom anti-reflective coating and said photo mask layer;

5 removing said middle etching stop layer which is at a bottom of said first trench and said partial dielectric hard mask layer;

removing said partial second dielectric constant dielectric layer to form a second trench in said second dielectric constant dielectric layer and removing said partial first dielectric constant dielectric layer to form
10 a third trench in said first dielectric constant dielectric layer, wherein said second trench and said third are connected with each other;

removing said cap layer which is at a bottom of said third trench and removing said middle etching stop layer which is at a partial bottom of said second trench;

15 forming a barrier layer on said second metal layer, said partial bottom of said second trench, a sidewall of said second trench, said bottom of said third trench, and a sidewall of said third trench;

forming a copper layer on said barrier layer and in said second trench and said third trench and filling of said second trench and said
20 third trench;

removing said partial copper layer to expose said second metal layer and making a surface of said third metal layer and said metal layer become a planar surface;

removing said barrier layer which is on said second metal layer
25 to expose said second metal layer; and

removing said second metal layer which is on said dielectric hard mask layer to expose said dielectric hard mask layer.

23. The method according to claim 22, wherein said second metal layer is titanium.

24. The method according to claim 22, wherein said second metal layer is titanium nitride.

25. The method according to claim 22, wherein said second metal layer is tantalum.

26. The method according to claim 22, wherein said second metal layer is tantalum nitride.

27. The method according to claim 22, wherein said second metal layer is aluminum.

28. The method according to claim 22, wherein said second metal layer is tungsten.

29. The method according to claim 22, wherein said middle etching stop layer is silicon nitride.

30. The method according to claim 22, wherein said middle etching stop layer is silicon carbon.

31. The method according to claim 22, wherein a material of said third metal layer is copper.

32. The method according to claim 22, wherein said barrier

layer is tantalum nitride/tantalum.

33. The method according to claim 22, wherein said barrier layer is titanium nitride/titanium.

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34. The method according to claim 22, wherein said dielectric hard mask layer is silicon carbon.

35. The method according to claim 22, wherein said
10 dielectric hard mask layer is silicon nitride.

36. The method according to claim 22, wherein a thickness of said second metal layer is about 50 to 500 anstroms.

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